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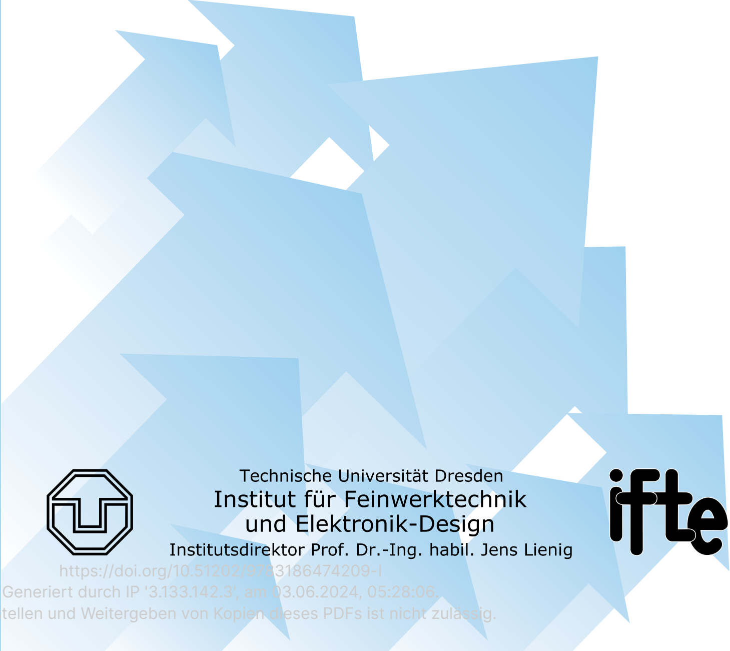
Constraint Propagation for Analog and Mixed-Signal Integrated Circuit Design



Technische Universität Dresden
Institut für Feinwerktechnik
und Elektronik-Design
Institutsdirektor Prof. Dr.-Ing. habil. Jens Lienig

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Technische Universität Dresden

Constraint Propagation for Analog and Mixed-Signal Integrated Circuit Design

Dipl.-Ing.

Andreas Krinke

von der Fakultät Elektrotechnik und Informationstechnik der
Technischen Universität Dresden

zur Erlangung des akademischen Grades

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While the design of digital integrated circuits (ICs) is largely automated, the design of analog/mixed-signal (AMS) ICs is still dominated by manual tasks. One of the biggest obstacles to further automation is the large number of constraints that have to be taken into account during AMS IC design. They are derived both from the specification and during the actual design process and must be fulfilled before production of the IC can begin. The aim of this work is to present our findings regarding the formalization of constraints and their propagation within the design hierarchy in order to make them visible and verifiable in all relevant cells. Constraints are integrated into the AMS IC design process so that they can be considered at all stages of the design. Our research enables the integration and consideration of constraints in all types of design tools—not only for AMS IC design, but after generalization for any design process.

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To make knowledge productive, we will have to learn to see both forest and tree.
We will have to learn to connect.
Peter F. Drucker

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Contents

Abbreviations

ADC	analog-to-digital converter
AMS	analog/mixed-signal
API	application programming interface
CAD	computer-aided design
CAS	computer algebra system
CLP	constraint logic programming
CMOS	complementary metal-oxide-semiconductor
CMP	chemical-mechanical planarization
CPLD	complex programmable logic device
CPU	central processing unit
CSP	constraint satisfaction problem
DAC	digital-to-analog converter
DBMS	database management system
DMA	direct memory access
DSP	digital signal processor
EDA	electronic design automation
ESD	electrostatic discharge
FPGA	field-programmable gate array
GDP	gross domestic product
GP	geometric programming
GPU	graphics processing unit
GSA	Global Semiconductor Alliance
HDL	hardware description language

HTTP	Hypertext Transfer Protocol
I/O	input/output
IC	integrated circuit
ID	identifier
IP	intellectual property
IPC	interprocess communication
JSON	JavaScript Object Notation
LDE	layout-dependent effect
LTE	Long Term Evolution
NoSQL	no (or not only) SQL
PDK	process design kit
RAK	rapid adoption kit
RAM	random-access memory
RDBMS	relational database management system (DBMS)
REST	representational state transfer
RF	radio frequency
RX	receiver
SA	simulated annealing
SOC	system on chip
SQL	structured query language
STI	shallow trench isolation
TX	transmitter
URL	uniform resource locator
VHDL	very high speed integrated circuit hardware description language
VLSI	very large scale integration
WFF	well-formed formula
WPE	well proximity effect

Selected Symbols

$\mathbb{B}$	Boolean domain
c	Constraint
C, C_i	Cell
C_p	Parent cell
D	Design state
$\mathcal{D}$	Set of all possible design states
E	Expression tree
F	Set of function symbols
G	Design hierarchy
I_i	Instance
M	Set of all possible constraint members
m_i	Constraint member
N	Net
Ω	Set of all possible values in a constraint function
O_X	Set of all global instances (occurrences) of cell X in the design
P	Set of predicate symbols
p	Predicate
Φ	Higher-order constraint function
φ	Constraint function
$\varphi*$	Transformed constraint function
Ψ	Set of design parameters
ψ	Design parameter

$\psi*$	Transformed design parameter
Q	Set of all possible constraint parameter values
q_i	Constraint parameter
S	Set of sorts
s	Shape
Σ	Signature of a many-sort predicative logic
σ	Sort
S_x	Set of electrically connected layout shapes
$\mathcal{T}$	Constraint type
T, T_i	Terminal
$T^{I_T}, T_i^{I_T}$	Instance terminal of instance I_T
X	Constraint context cell
$\mathcal{X}$	Set of all cells in the design

Abstract

While the design of digital integrated circuits (ICs) is largely automated, the design of analog/mixed-signal (AMS) ICs is still dominated by manual tasks. One of the biggest obstacles to further automation is the large number of constraints that have to be taken into account during AMS IC design. They are derived both from the specification and during the actual design process and must be fulfilled before production of the IC can begin. Current IC design tools hardly support working with constraints—they are either not formally described and are therefore only available as export knowledge, or they are not visible in all cells in which they must be considered.

This thesis addresses three selected, practically relevant problems of constraint management during AMS IC design: (1) formal description of constraints and their classification, (2) propagation of constraints within the design hierarchy so that they are visible and verifiable in all relevant cells, and (3) influence of constraints on the modeling and storage of design data. By implementing solutions to all three problems, the comprehensive and consistent consideration of constraints in the entire design hierarchy and flow is made possible, thereby overcoming the obstacle described above.

The objective of this work is to formalize constraints and integrate them into the AMS IC design process so that they can be considered at all stages of the design. Experimental investigations show the practical suitability of the methods even for complex circuits. Our findings enable the integration and consideration of constraints in all types of design tools—not only for AMS IC design, but after generalization also for any design process.

Kurzfassung

Der Entwurf digitaler integrierter Schaltungen (ICs) ist weitestgehend automatisiert. Im Gegensatz dazu wird der Entwurf analoger und gemischt analog/digitaler AMS-ICs noch immer von manuellen Arbeiten dominiert. Eines der größten Hindernisse für die weitere Automatisierung ist die große Zahl von Randbedingungen, die beim Analogentwurf berücksichtigt werden müssen. Diese ergeben sich sowohl aus der Spezifikation als auch während des eigentlichen Entwurfs und müssen erfüllt sein, bevor die Herstellung des Schaltkreises beginnen kann. Aktuelle Entwurfswerkzeuge unterstützten die Arbeit mit Randbedingungen kaum – entweder sie sind nicht formal beschrieben und liegen somit nur als Expertenwissen vor, oder sie sind nicht in allen Zellen sichtbar, in denen sie beachtet werden müssen.

In dieser Arbeit werden drei ausgewählte, praktisch relevante Problemstellungen der Verwaltung von Randbedingungen beim Entwurf von AMS-ICs bearbeitet: (1) die formale Beschreibung von Randbedingungen und ihre Klassifikation, (2) die Propagierung von Randbedingungen innerhalb der Entwurfshierarchie, so dass sie in allen relevanten Zellen sicht- und verifizierbar sind, sowie (3) der Einfluss von Randbedingungen auf die Modellierung und Speicherung von Entwurfsdaten. Durch die Implementierung von Lösungen für alle drei Probleme wird die umfassende und konsistente Berücksichtigung von Randbedingungen in der gesamten Entwurfshierarchie und in allen Teilen des Entwurfsprozesses ermöglicht und damit das oben beschriebene Hindernis überwunden.

Das Ziel dieser Arbeit besteht darin, Randbedingungen zu formalisieren und in den Entwurfsprozess von AMS-ICs zu integrieren, so dass sie in allen Phasen des Entwurfs berücksichtigt werden können. Experimentelle Untersuchungen zeigen die Praxistauglichkeit der Methoden auch für komplexe Schaltungen. Die Erkenntnisse ermöglichen die Integration und Berücksichtigung von Randbedingungen in allen Arten von Entwurfswerkzeugen – nicht nur für den Entwurf von AMS-ICs, sondern nach Verallgemeinerung auch für beliebige Entwurfsprozesse.